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STATUTORY DECLARATION

I, Ho Jin PARK, a citizen of the Republic of Korea and a staff member of Y.H.KIM INTERNATIONAL PATENT & LAW OFFICE specializing in "LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF", do hereby declare that:

(1) I am conversant with the English and Korean languages and a competent translator thereof.

(2) To the best of my knowledge and belief, the following is a true and correct translation of the Priority Document (No. P2000-76850) in the Korean language already filed with Korean Industrial Property Office on December 15, 2000.

Signed this 18th day of May, 2004

Ho Jin PARK

#12

PATENT APPLICATION

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Patent Attorney

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ABSTRACTS

[Abstract]

The present invention relates to a liquid crystal display device and a driving method thereof that detects a presence and a frequency range of an input signal applied to the liquid crystal display. The liquid crystal display device according to the present invention comprises a signal presence determiner for detecting an application of an input signal from an interface. The signal presence determiner includes an oscillator for generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal, a period detector for comparing a data enable signal from the exterior thereof with the reference clock to output a period of the input signal using a detection reference signal and the pre-synchronizing signal, a period comparator for comparing a period range between a desired maximum value and a desired minimum value of the input signal, and signal presence/absence comparing means for determining a presence/absence of the input signal in accordance with a number of pulses of the input signal detected within a period range between the maximum value and the minimum value during applying the detection reference signal. According to the present invention, with an addition of the period comparator, a presence/absence and a frequency range of an input signal from the interface can be detected, thereby supporting various frequency ranges of a liquid crystal module for a monitor.

[Representative drawing]

Fig. 6

SPECIFICATION

[Title of the invention]

LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

[Brief description of the drawings]

Fig. 1 is a block diagram showing a conventional liquid crystal display.

Fig. 2 is a schematic block diagram showing the timing controller shown in Fig. 1.

Fig. 3 is a schematic flow chart representing a conventional signal presence determiner shown in Fig. 2.

Fig. 4 is a waveform diagram representing a process of generating a judgment signal from the signal presence determiner shown in Fig. 3.

Fig. 5 shows a multiplexor provided at the timing controller shown in Fig. 3.

Fig. 6 is a schematic flow chart representing a signal presence determiner according to the present invention.

Fig. 7 is a timing diagram representing a process of generating a judgment signal from the signal presence determiner shown in Fig. 6.

Fig. 8 shows the period detector shown in Fig. 6.

Fig. 9 shows the period comparator shown in Fig.6.

Fig. 10 shows the period comparator shown in FIG. 7.

Detailed descriptions of the reference number

2: liquid crystal panel 10: interface

12, 34: timing controller 14: power voltage generator

16: reference voltage generator

18: data driver 20: gate driver

22, 30: control signal generator
24, 32: data signal generator
26: oscillator
28: signal presence determiner
40: multiplexor 42, 50: input signal
41, 52: pre-synchronizing signal
44: frequency comparator
46, 58: signal presence comparator
48, 60: signal absence comparator
54: period detector 56: period comparator
62: signal presence/absence comparator
70, 72: comparator

[Detailed description of the invention]

[Object of the invention]

[Technical field including the invention and prior art therein]

This invention relates to a method of driving a liquid crystal display, and more particularly to a method of driving a liquid crystal display that detects a presence and a frequency range of an input signal applied to the liquid crystal display.

Generally, a liquid crystal display (LCD) has been employed a notebook PC, an office automation equipment and an audio/video equipment, etc. owing to advantages of a small dimension, a thin thickness and a low power consumption. In particular, an active matrix liquid crystal display using thin film transistors (TFTs) as switching devices is suitable for displaying a dynamic image.

Fig. 1 is a block diagram showing a conventional liquid crystal display.

Referring to Fig. 1, an interface 10 receives a data

(RGB data) and control signals (e.g., an input clock, a horizontal synchronizing signal, a vertical synchronizing signal and a data enable signal) inputted from a driving system such as a personal computer and supplies them to a timing controller 12. A low voltage differential signal (LVDS) interface and a transistor-transistor logic (TTL) interface are largely used for a data and control signal transmission from the driving system. Such interfaces may be integrated into a single chip along with the timing controller 12.

The timing controller 12 uses a control signal through the interface 10 to generate control signals for driving a data driver 18 consisting of a plurality of drive ICs and a gate driver 20 consisting of a plurality of gate drive ICs. Also, the timing controller 12 transfers a data from the interface 10 to the data driver 18.

A reference voltage generator 16 generates reference voltages of a digital to analog converter (DAC) used in the data driver 18. These reference voltages are set by a manufacturer based on a transmissivity to voltage characteristic of a liquid crystal panel.

The data driver 18 selects reference voltages of an input data in response to control signals from the timing controller 12 and supplies the selected reference voltages to the liquid crystal display panel 2, thereby controlling a rotation angle of the liquid crystal.

The gate driver 20 makes an on/off control of the thin film transistors arranged on the liquid crystal panel 2 in response to the control signals inputted from the timing controller 12, and allows the analog image signals from the data driver 18 to be applied to each pixel connected to each TFT. A power voltage generator 14 supplies an

operation voltage to each element. The power voltage generator 14 also generates a common electrode voltage and applies it to the liquid crystal panel 2.

Fig. 2 is a schematic block diagram showing the timing controller shown in Fig. 1.

Referring to Fig. 2, the timing controller 34 includes a control signal generator 22 receiving a horizontal synchronizing signal, a vertical synchronizing signal, and a timing synchronizing signal of a data enable and a clock pulse from the interface 10 to generate control signals, which are supplied to the data driver 18 and the gate driver 20, a data signal generator 32 receiving and arranging data (R, G, B) from the interface 10 to supply them to the data driver 18, a signal presence determiner 28 for detecting an application of various control signals from the interface 10, and a oscillator 26 for supplying a reference signal with a predetermined frequency to the signal presence determiner 28.

The control signal generator 30 receives a horizontal synchronizing signal, a vertical synchronizing signal, a data enable signal, and a clock signal to generate various control signals for driving the liquid crystal panel, and supplies the control signals to the data driver 18 and the gate driver 20. Herein, the vertical synchronizing signal represents a time required for displaying one frame field. The horizontal synchronizing signal represents a time required for displaying one line of the field. Thus, the horizontal synchronizing signal includes pulses corresponding to the number of pixels included in one line. The data enable signal represents a time supplying the pixel with a data.

The data signal generator 32 receives and rearranges a

data (R, G, B) from the interface 10 to supply them to the data driver 18 so that the data can be supplied to the liquid crystal panel 2.

The oscillator 26 generates a desired reference clock and makes a frequency division of the reference clock to apply a pre-synchronizing signal having the same frequency as an input signal to the signal presence determiner 28.

An operation of the signal presence determiner 28 will be now described with reference to Fig. 3. The signal presence determiner 28 includes a frequency comparator 44 receiving an input signal 42 and a pre-synchronizing signal 41, and a signal presence comparator 46 and a signal absence comparator 48 for checking a variation in a frequency signal to be compared.

The frequency comparator 44 receives the input signal 42 from the interface 10, and also the pre-synchronizing signal 41 having the same frequency as the input signal 42 from the oscillator 26. The frequency comparator 44 compares a frequency of the pre-synchronizing signal 41 with that of the input signal 42. In other words, the frequency comparator 44 determines whether when the pre-synchronizing signal has a frequency of 60Hz, the detected frequency of the input signal during a desired period is fallen within a ±5Hz range of the pre-synchronizing signal 41. Then, the input signal 42 is applied to the signal presence comparator 46 to check a variation in frequency. The signal presence comparator 46 compares the input signal 42 with the pre-synchronizing signal 41 like an A section in Fig. 4 to apply a low-state judgment signal indicating to be an effective signal input to the control signal generator 30 when a repetition number of high state or low state of the input signal 42 is larger than a set value N.

The control signal generator 30 having received a low-state judgment signal is supplied with an input signal from the interface 10. The rest operation conforms to a general operation of generating control signals.

However, when the input signal 42 has a frequency of more than ±5Hz of the pre-synchronizing signal 41, the input signal is applied to the signal absence comparator 48 to check a variation of frequency.

The signal absence comparator 48 compares the input signal 42 with the pre-synchronizing signal 41 like a B section in Fig. 4 to apply a high-state judgment signal indicating to be an ineffective signal input to the control signal generator 30 when a repetition number of high state or low state of the input signal 42 is smaller than a set value N.

The control signal generator 30 having received a high-state judgment signal receives the pre-synchronizing signal 41 from the oscillator 26 to display a full black, a full white or certain picture information on the liquid crystal display panel 2. To this end, the control signal generator 30 includes a multiplexor (MUX) 40 as shown in Fig. 5.

Referring to Fig. 5, the MUX 40 receives a pre-synchronizing signal, an input signal and a judgment signal, and selectively output any one of the pre-synchronizing signal and the input signal as a synchronizing signal in accordance with an input state of the judgment signal. Herein, the MUX 40 outputs an input signal when a low-state judgment signal is inputted, while it outputs a pre-synchronizing signal when a high-state judgment signal is inputted. Then, the control signal generator 30 generates and outputs various control signals based on an input

signal or a synchronizing signal from the MUX 40. Further, data is stored in advance in a storage device such as ROM, which is integrated within a data signal generator block of the timing controller 34, or exterior flash memory.

As described above, the conventional method of detecting a presence of signal can detect a presence of signal only for a certain frequency of the input signal, not a frequency range of the input signal. Accordingly, the conventional detecting method cannot support various frequency range of a liquid crystal module for monitor.

[Technical subject matter to be solved by the invention]

Accordingly, it is an object of the present invention to provide a liquid crystal display and a driving method thereof that detect a presence and a frequency range of an input signal applied to the liquid crystal display.

[Configuration and operation of the invention]

In order to achieve the object of the invention, a liquid crystal display device according to the present invention includes a signal presence determiner for detecting an application of an input signal from an interface, wherein the signal presence determiner includes an oscillator for generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal, a period detector for comparing a data enable signal from the exterior thereof with the reference clock to output a period of the input signal based on a detection reference signal and the pre-synchronizing signal, a period comparator for comparing a period range between a desired maximum value and a desired

minimum value of the input signal, and a signal presence/absence determiner for determining a presence/absence of the input signal in accordance with a number of pulses of the input signal detected within a period range between the maximum value and the minimum value during applying the detection reference signal.

A method of driving a liquid crystal display device including a timing controller having a signal presence determiner for detecting a presence of an input signal from an interface, according to the present invention, the method including the steps of: generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal, comparing a data enable signal from the exterior with the reference clock to output a period of an input signal using a detection reference signal and the pre-synchronizing signal, comparing a period range between a desired maximum value and a desired minimum value of the input signal, and determining a presence/absence of the input signal in accordance with a number of pulses of the input signal detected within a period range between the maximum value and the minimum value during applying the detection reference signal.

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings.

The preferred embodiments of the present invention will now be described with reference to Figs. 6 to 10.

Fig. 6 is a flow chart representing a signal presence determiner according to a preferred embodiment of the

present invention.

Referring to Fig. 6, the signal presence determiner includes a period detector receiving an input signal 50 and a pre-synchronizing signal 52, a period comparator 56 for comparing the detected period range with a period range between a set maximum period and a set minimum period, a signal presence comparator 58 and a signal absence comparator 60 for determining whether the period larger or smaller than the set period during P input signals is continuously inputted, and a signal presence/absence comparator 62 for finally determining a presence of a signal.

The period detector 54 includes two input terminals and two output terminals as shown in Fig. 8.

Referring to Fig. 8, the period detector 54 receives and compares the input signal 50 from the interface 10 and the pre-synchronizing signal 52 from the oscillator 26 as shown in Fig. 7, and outputs a period signal P_{VSYNC} and a detection reference signal REF_{VSYNC}.

The period comparator 56 includes a first comparator 70 and a second comparator 72, each having two input terminals and one output terminal, as shown in Fig. 9.

Referring to Fig. 9, the first comparator 70 determines whether the period signal P_{VSYNC} is smaller than the set maximum (MAX) period. Then, the second comparator 72 determines whether the period signal P_{VSYNC} is larger than the set minimum (MIN) period. The period comparator 56 provides the signal presence comparator 58 with an output signal COM when the period signal is fallen within a range between the maximum period and the minimum period, and the signal absence comparator 60 with an output signal COM when the period signal is larger than the maximum period or

smaller than the minimum period.

Referring to Fig. 10, the signal presence comparator 58 includes two input terminal and one output terminal.

The signal presence comparator 58 receives the input signal from the period comparator 56 and the detection reference signal REF_{VSYNC}.

The signal presence comparator 58 receives a period signal within a range between the set MAX period and MIN period from the period comparator 56 and determines to be a presence signal when the number of pulses having continuous 0 or 1 value during the detection reference signal REF_{VSYNC} is larger than a set P value. Then, the presence signal is applied to the signal presence/absence comparator 62. Further, the signal presence comparator 58 receives a period signal larger than the set MAX or less than the set MIN period from the period comparator 56 and determines to be a absence signal when the number of pulses having continuous 0 or 1 value during the detection reference signal REF_{VSYNC} is larger than a set P value. Then, the absence signal is applied to the signal presence/absence comparator 62.

The signal presence/absence comparator 62 receives a signal DET determined at the signal presence comparator 58 and the signal absence comparator 60, and supplies the signal DET to the control signal generator 30.

The input signal 50 determined to be the presence signal at the signal presence/absence comparator 62 takes a normal operation, but the input signal 50 to be the absence signal is applied to the control signal generator to receive a pre-synchronizing signal from the oscillator 26, thereby displaying a full black, a full white or a certain pre-stored data on the liquid crystal panel. To this end,

the control signal generator 30 includes a multiplexor (MUX) 40 as shown in Fig. 5.

Referring to Fig. 5, the MUX 40 receives a pre-synchronizing signal, an input signal and a judgment signal, and selectively output any one of the pre-synchronizing signal and the input signal as a synchronizing signal in accordance with an input state of the judgment signal. Herein, the MUX 40 outputs an input signal when a low-state judgment signal is inputted, while it outputs a pre-synchronizing signal when a high-state judgment signal is inputted. Then, the control signal generator 30 generates and outputs various control signals based on an input signal or a synchronizing signal from the MUX 40. Further, data is stored in advance in a storage device such as ROM, which is integrated within a data signal generator block of the timing controller 34, or exterior flash memory.

[Effect of the invention]

As described above, according to a liquid crystal display device and a driving method thereof of the present invention, the signal presence/absence determiner of the timing controller further includes the period comparator, thereby detecting a presence/absence of an input signal from the interface. Furthermore, a frequency range of the input signal is detected, so that it becomes possible to support various frequency ranges of a liquid crystal module for a monitor.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the preferred embodiments, but rather that various changes or

modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

[What is claimed is]

1. A liquid crystal display device including a timing controller having a signal presence determiner for detecting a presence of an input signal from an interface, wherein the signal presence determiner comprising:

an oscillator for generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal;

a period detector for comparing a data enable signal from the exterior thereof with the reference clock to output a period of the input signal using a detection reference signal and the pre-synchronizing signal;

a period comparator for comparing a period range between a desired maximum value and a desired minimum value of the input signal; and

a signal presence/absence determiner for determining a presence/absence of the input signal in accordance with a number of pulses of the input signal detected within a period range between the maximum value and the minimum value during applying the detection reference signal.

2. The liquid crystal display device as claimed in claim 1, wherein the period range between the maximum value and the minimum value of the period comparator is adjustable by a user.

3. The liquid crystal display device as claimed in claim 1, wherein the number of pulses of the signal presence/absence determiner is adjustable by a user.

4. A method of driving a liquid crystal display device

including a timing controller having a signal presence determiner for detecting an application of an input signal from an interface, the method comprising the steps of:

generating a reference clock having the same frequency as a horizontal synchronizing signal and a pre-synchronizing signal having the same frequency as a vertical synchronizing signal;

comparing a data enable signal from the exterior with the reference clock to output a period of the input signal with the aid of a detection reference signal and the pre-synchronizing signal;

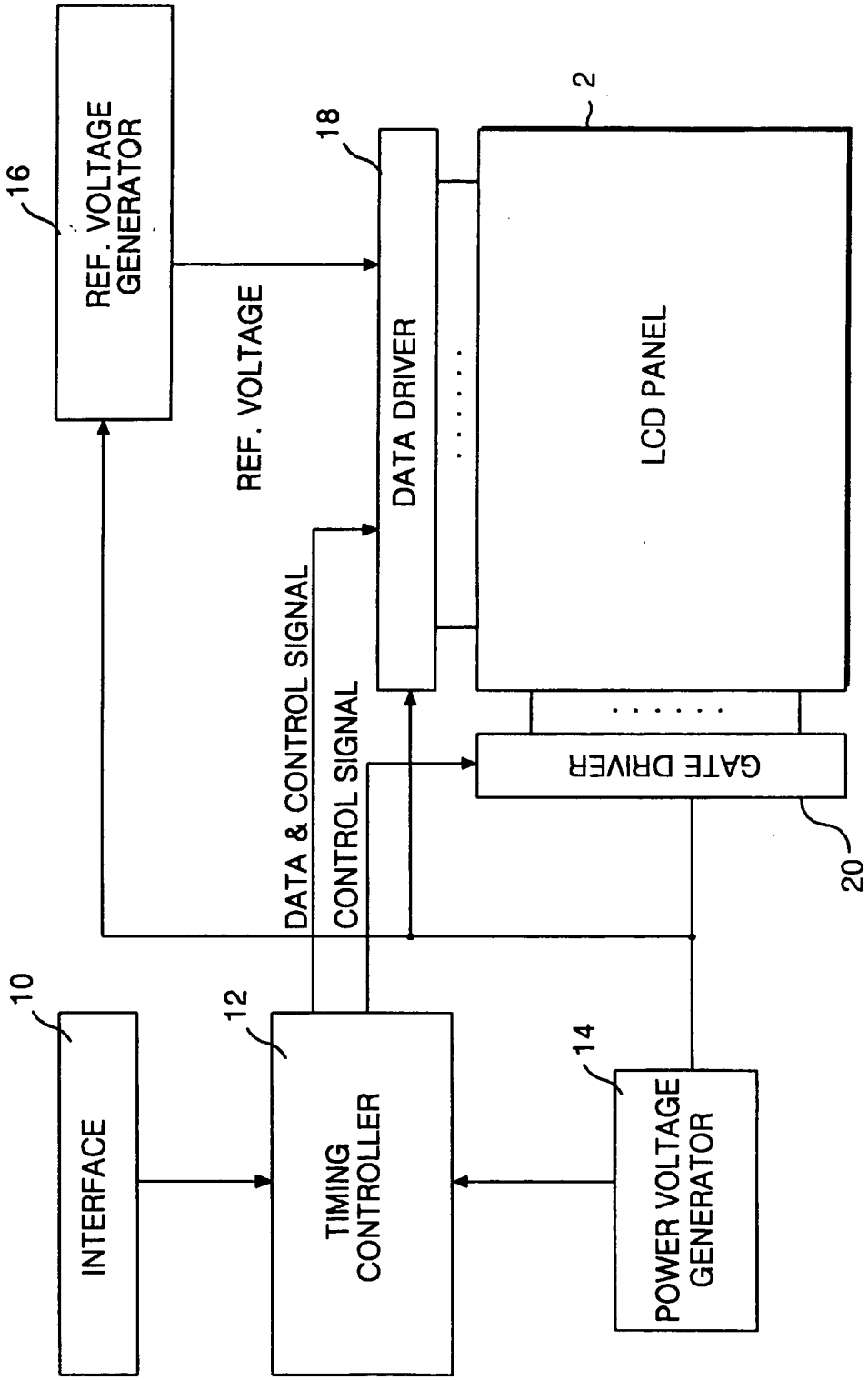
comparing a period range between a desired maximum value and a desired minimum value of the input signal; and

determining a presence/absence of the input signal in accordance with a number of pulses of the input signal detected within a period range between the maximum value and the minimum value during applying the detection reference signal.

5. The method as claimed in claim 4, wherein the period range between the maximum value and the minimum value is adjustable by a user.

6. The method as claimed in claim 4, wherein the number of pulses of the input signal is adjustable by a user.

FIG. 1



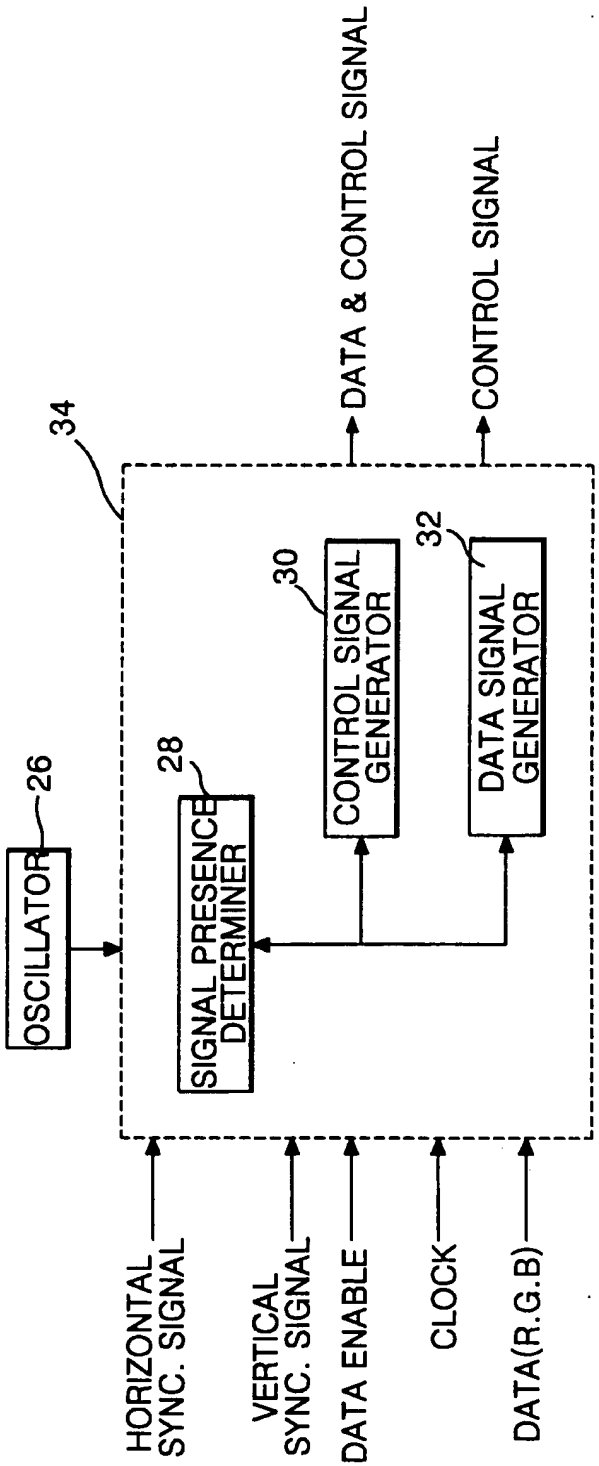


FIG.2

FIG.3

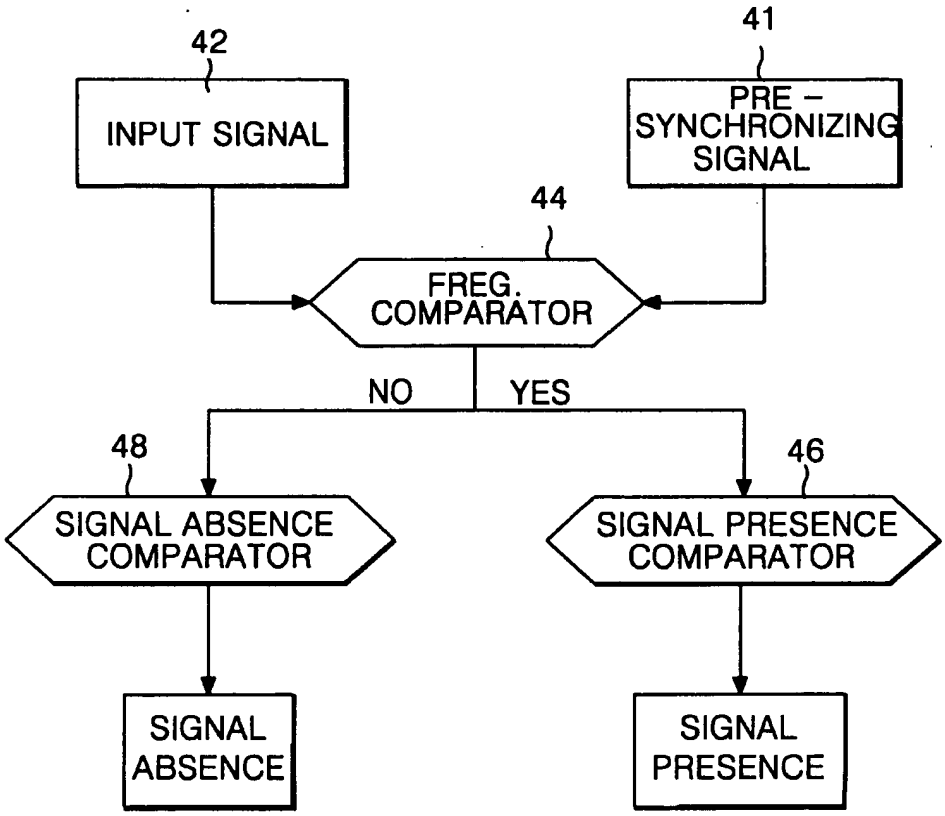


FIG. 4

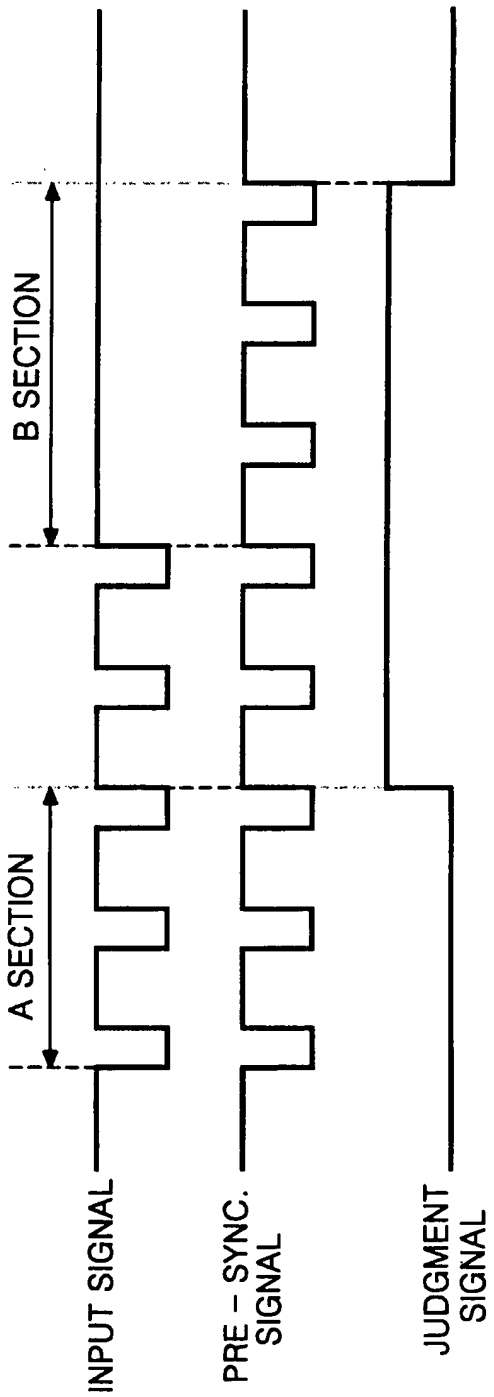


FIG.5

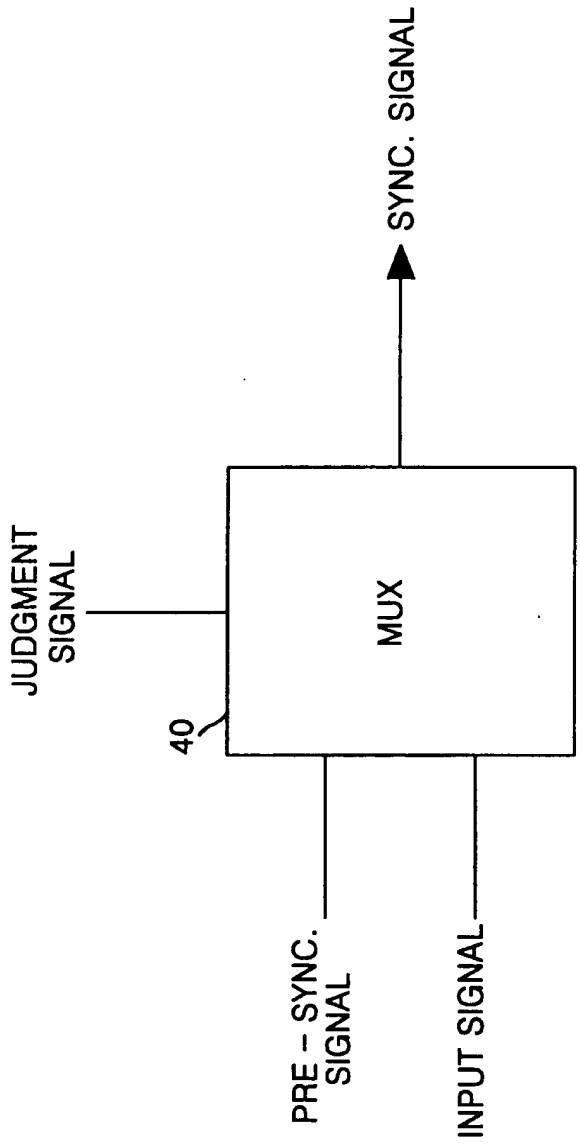


FIG.6

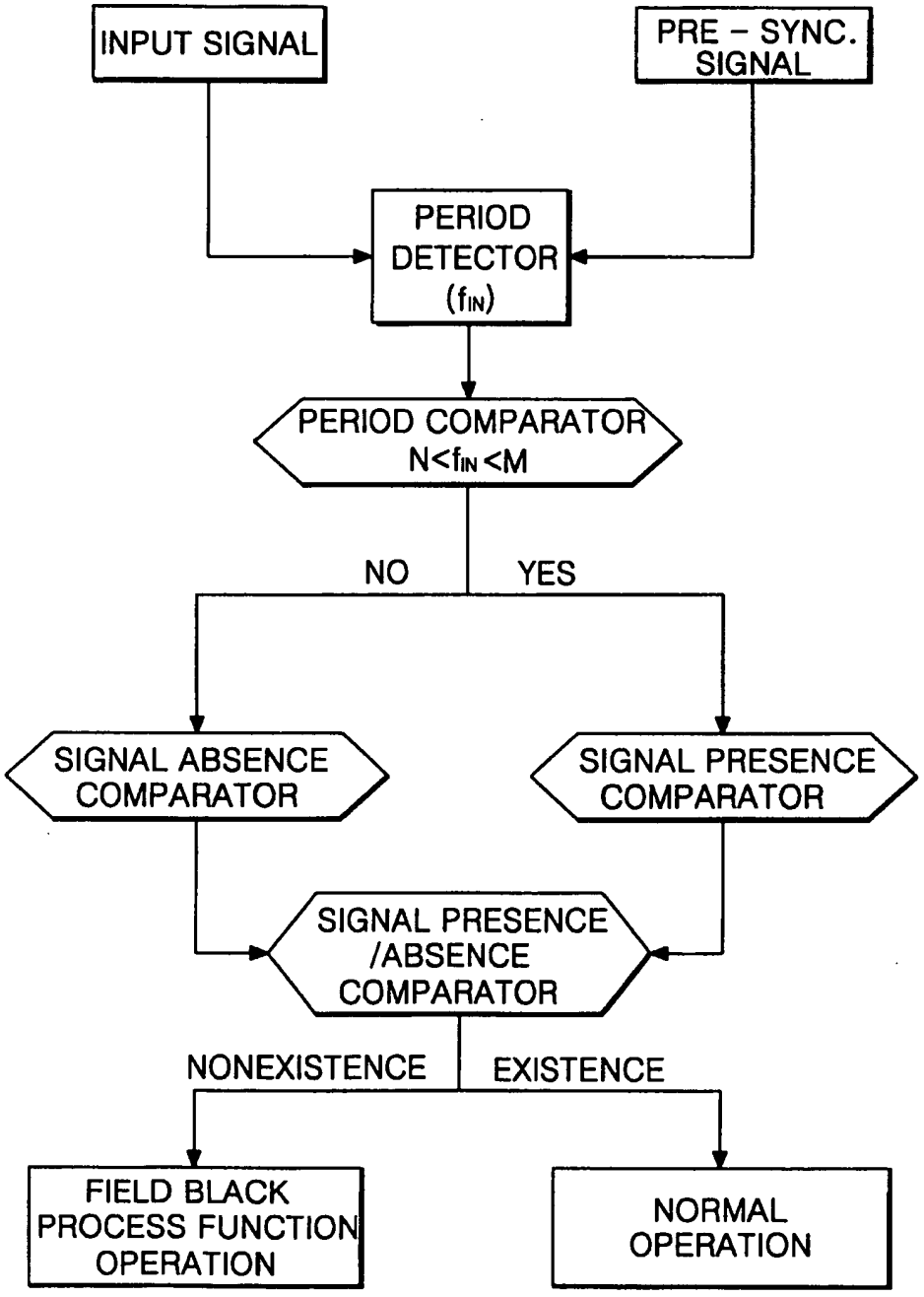


FIG.7

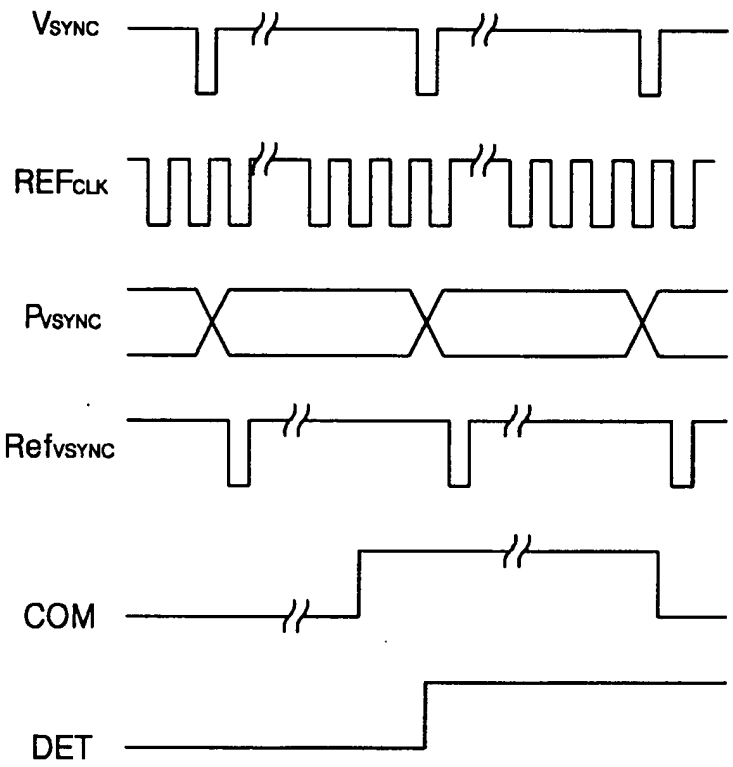


FIG.8

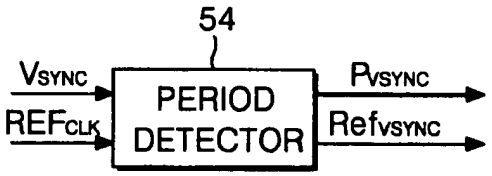


FIG.9

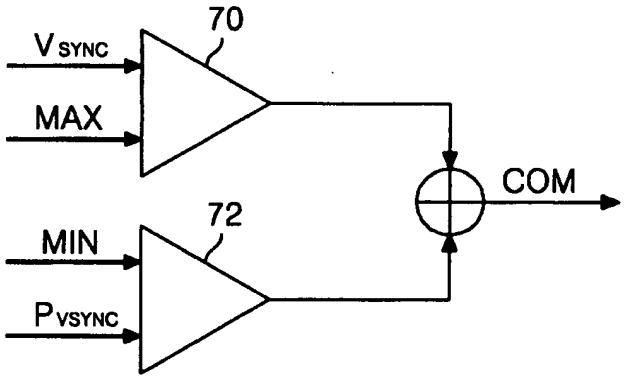


FIG.10